MEETING PCB TECHNICAL CLEANLINESS CHALLENGES WITH ALTAIR® POLLEX™

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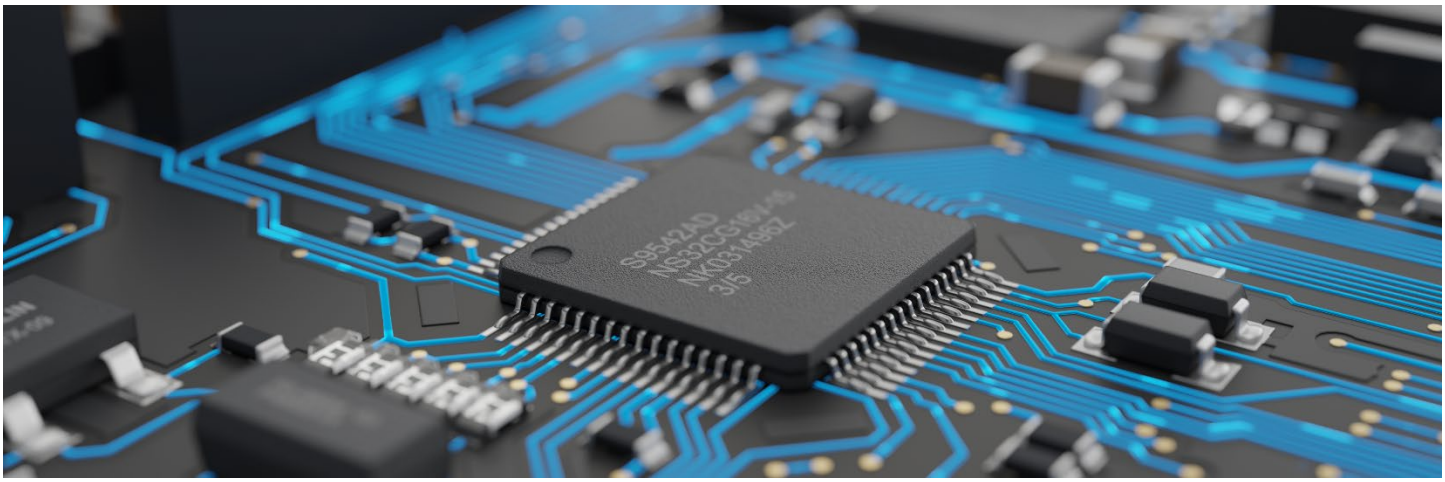


Ensuring Technical Cleanliness for PCB Design Verification

Technical cleanliness refers to the level of purity required in production to ensure the reliable performance of products or systems. It involves controlling the type, number, and size of particles, impurities, flux residues, and contaminants that can impact the behavior, reliability, and lifespan of a product.

Industries have different levels of sensitivity to particles and contaminants and subsequently different requirements for printed circuit board (PCB) impurity control and PCB particle control. For example, medical devices and automotive and aerospace components typically require higher levels of technical cleanliness than consumer goods. The degree of technical cleanliness sensitivity also depends upon the application.

In the automotive sector, technical cleanliness is crucial. Inaction can potentially impact automotive OEMs, tier-one suppliers, and other partners in the following ways:

1. **Reliability and Performance:** The presence of PCB contaminants in critical components such as engine parts, sensors, and electronic systems can lead to malfunctions, reduced performance, and even catastrophic failures. Technical cleanliness reduces the risk of such failures and improves product reliability and performance.

2. **Cost:** Contamination-related failures can result in expensive warranty claims, recalls, and customer dissatisfaction.

3. **Non-Compliance with Standards and Regulations:** Many industries, including the automotive sector, have stringent cleanliness standards and regulations that must be met. Non-compliance can lead to legal issues, penalties, and market entry barriers.

4. **Product PCB Lifespan:** Contaminants such as conductive particles can cause components to malfunction and degrade prematurely, leading to a reduced lifespan. Technical cleanliness practices—such as proper cleaning procedures and maintenance—help to improve the durability of components and systems, extending their life, reducing replacement costs, and reducing environmental impact.

5. **Supplier Relationships:** Automotive OEMs and tier-one suppliers often rely on a network of suppliers to provide various components and subsystems. Implementing technical cleanliness standards and requirements helps establish strong supplier relationships based on trust, quality, and adherence to standards.

While technical cleanliness is particularly important in the automotive industry, it's also relevant in other sectors such as aerospace, electronics, medical devices, and manufacturing.

To achieve technical cleanliness, manufacturers may use various cleaning and filtration methods. They may also implement measures and standards to prevent contamination during the manufacturing and handling processes. These standards and guidelines are established by industry associations or government agencies to ensure consistency and quality in manufacturing processes. These standards can also be applied during the design phase, which is the subject of this whitepaper.

ZVEI Technical Cleanliness Standards

Many companies have created and developed standards for technical cleanliness based on national and international regulations. This has led to a variety of requirements, norms, and specifications. Many of these have proven difficult to meet, prompting industry organizations to refine those requirements for their own industries.

The Zentralverband Elektrotechnik- und Elektronikindustrie e. V. (ZVEI), a German trade association that represents the electrical and electronic industry in the country, has established a set of guidelines to ensure technical cleanliness in electronic manufacturing. Those guidelines, titled "Technical Cleanliness in Electrical Engineering," are based on the VDA 19.1 and VDA 19.2 standards for automotive systems.

The ZVEI technical cleanliness standard defines a technical cleanliness classification system for PCBs based on the number and size of contaminants present on a board's surface. It covers various domains that affect technical cleanliness, including:

- Manufacturing
- Packaging
- Transport of electronic components and devices

The standard's aim is to define and implement quantifiable component cleanliness analysis.

Potential malfunctions particles can cause, but are not limited to, the following malfunctions:

- Short circuit
- Reduced creepage and clearance distance
- Mechanical obstruction
- Increased or reduced power
- Increase in leakage currents
- Pin-to-pin shortage

It's important to note that the ZVEI standard is not a legal requirement, but is commonly used as guidelines by companies in the electronics industry.

The following table from the ZVEI guidelines (Table 1) shows the level of cleanliness that can be achieved without special cleaning processes. The particle counts listed are empirical values from observation:

Empirical Particle Data from Assembled PCBs[2] per 1000 cm² Surface, Based on Particle Class

Particle size [µm]	Size classes	All particles	Metallic particles[1]
50 ≤ x < 100	E	14500	1000
00 ≤ x < 150	F	2500	250
150 ≤ x < 200	G	800	90
200 ≤ x < 400	H	600	110
400 ≤ x < 600	I	70	17
600 ≤ x < 1000	J	20	13
1000 ≤ x	K	6	2

1) The count of metallic particles can be significantly higher on connectors with metal housings or heat sinks.
2) Without any cleaning process

Table 1 – Empirical data for PCB classification from electronics manufacturing cluster
Source – ZVEI guideline Technical Cleanliness in Electrical Engineering

Particle Tolerance and PCB Reliability

Table 1 shows that while it's possible to achieve a high level of technical cleanliness in the PCB manufacturing process, it's difficult to eliminate the presence of very small particles on a board's surface. Furthermore, for devices that must operate in particle-rich environments subject to humidity and vibration—as is the case with automobiles, for example—it's generally not economically feasible to prevent the penetration of very small particles into a PCB's housing. Vibration can cause these particles to move about the surface of the PCB, thereby creating a risk of a short circuit if such a particle is large enough to connect two of the board's conducting traces.

It's therefore important that PCBs be designed to tolerate the presence of these very small particles so they can reliably function in their normal operating environment.

Until recently, ensuring such tolerance has strictly been a matter of inspection during the prototyping phase of PCB production. Typically, a manufactured prototype is manually inspected under a microscope to identify potential risk areas and recommend measures for mitigation of these risks. Mitigation measures may include modifications to the board's design to increase the separation between contacts, applying coatings to portions of the board, or the use of special housings. In any case, this manual inspection procedure generates not just an iteration of the PCB design process, but of the board prototyping process as well.

Today, PCB technical cleanliness tools can help implement the ZVEI standard by comparing the geometries of layout structures with the representative particles. Using such tools allows the PCB design engineer to solicit a technical cleanliness review and implement risk mitigation recommendations before sending a design for prototyping. Making use of this innovation can greatly reduce production costs.

Technical Cleanliness in Altair® PollEx™

Altair® PollEx™ enables technical cleanliness verification at the design stage to help manufacturers improve PCB reliability and shorten design cycles with the following capabilities:

- Automatically inspects the design for cleanliness (particle tolerance) issues, such as shorts or solder bridges.
- Detects the areas where such risk exists and computes the total risk area per particle size.
- Highlights risk areas and the objects (pads or solder mask) affected for easy review.
- Generates documentation that specifies the cleanliness requirements for the design and the ZVEI cleanliness class of the design.

Defining Analyses by Particle Size

Figure 1 shows the Technical Cleanliness Input and Constraints window in the PollEx user interface:

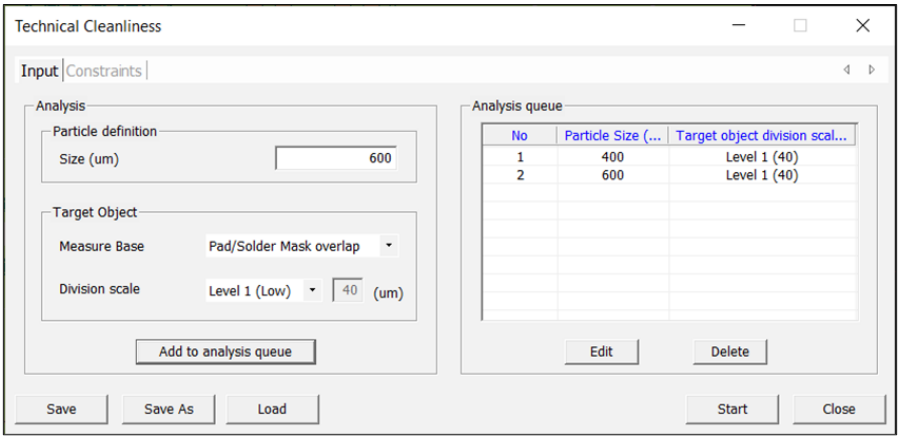


Figure 1 – PollEx Technical Cleanliness Window

In the Technical Cleanliness window, users can set:

- The size of the particle
- The target objects for the cleanliness check. This can be:
  - Pads
  - Solder mask
  - Pad/solder mask overlap
- The grid to apply for the target objects' division (Division scale)

The division scale is needed to measure the distance between the target objects and check if this distance is less or greater than the particle size. The tool offers three pre-set values (40, 20 and 5 microns) for this division scale, as well as the option for the user to specify a different value. The smaller the division scale, the greater the accuracy, but at the expense of longer runtime.

Several analyses may be queued to run as a batch. The user simply defines the particle size, measure base, and division scale for a given analysis in the Analysis window and then clicks the "Add to analysis queue" button to put the analysis in the queue.

The tool will calculate the area between any two objects that can be connected by a particle of the selected size. The larger the area, the greater the risk that the particle can cause a short circuit and potentially harm the board or affect its functionality.

Figure 2 illustrates a critical area between two objects and how the total risk area per particle size is computed. If the distance between two target objects is less than the particle size, the tool will compute the area enclosed by the target objects and lines referring to the particle size connecting these objects.

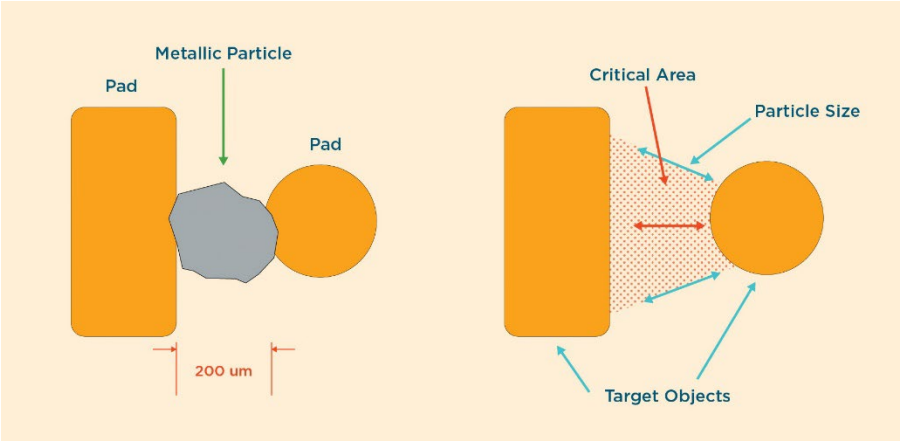


Figure 2 – Illustration of a Metallic Particle and Critical Area

Controlling Analysis Scope for Faster, More Cost-Effective PCB Cleanliness Verification

The PollEx Technical Cleanliness workflow lets users generate results faster by defining constraints and fine-tuning analyses to:

- Exclude unassigned nets from the check
- Exclude pins on components from the check
- Exclude same nets
- Exclude areas covered with coating layers (user-defined layers on top and bottom side of the board)
- Target nets: These can be all the nets in the design (default), or specific nets defined by groups and identified by a string (prefix, mid-string, or suffix)

Exclusions save users' time by suppressing analysis of areas of the board where protection has already been accounted for, or that are not currently of interest to the user. Using these constraints reduces runtime, false alarms, and the number of results the user must review in post-processing. Figure 3 shows the Constraints tab in PollEx Technical Cleanliness:

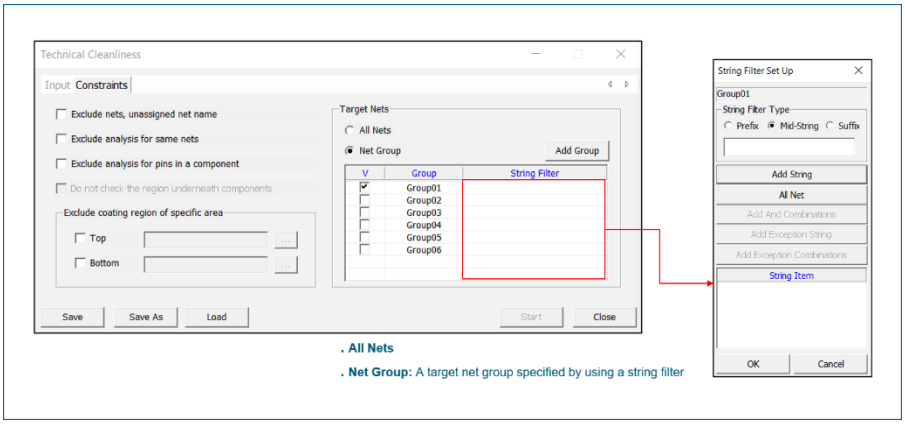


Figure 3 – Constraints tab in PollEx Technical Cleanliness Verification

Obtaining Analysis Results

Once the queued analyses runs and the technical cleanliness check is completed, engineers and designers can view results in a report (Figure 4) that includes:

- Target objects with a separation distance smaller than the particle size (for each particle size)
- Critical area per board side (top and bottom) by particle size

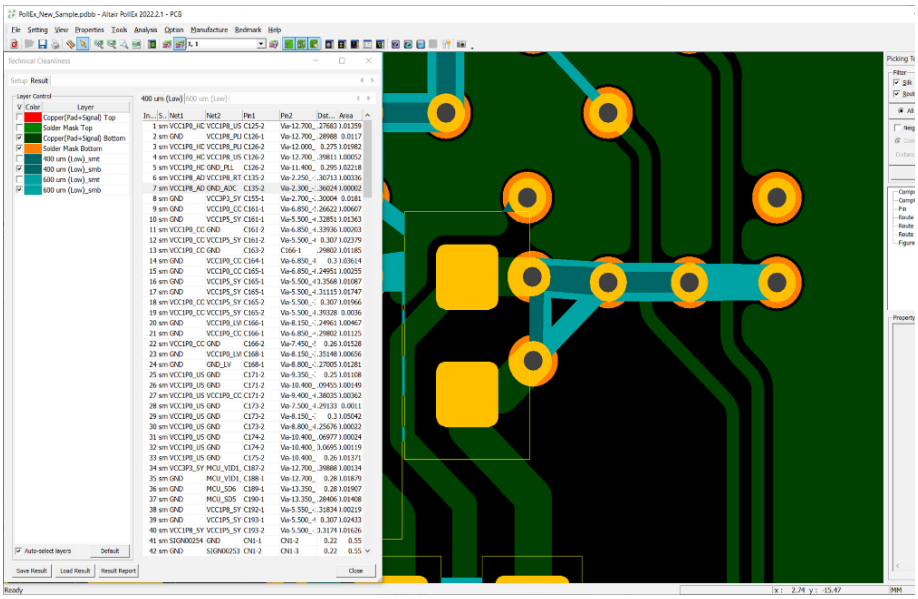
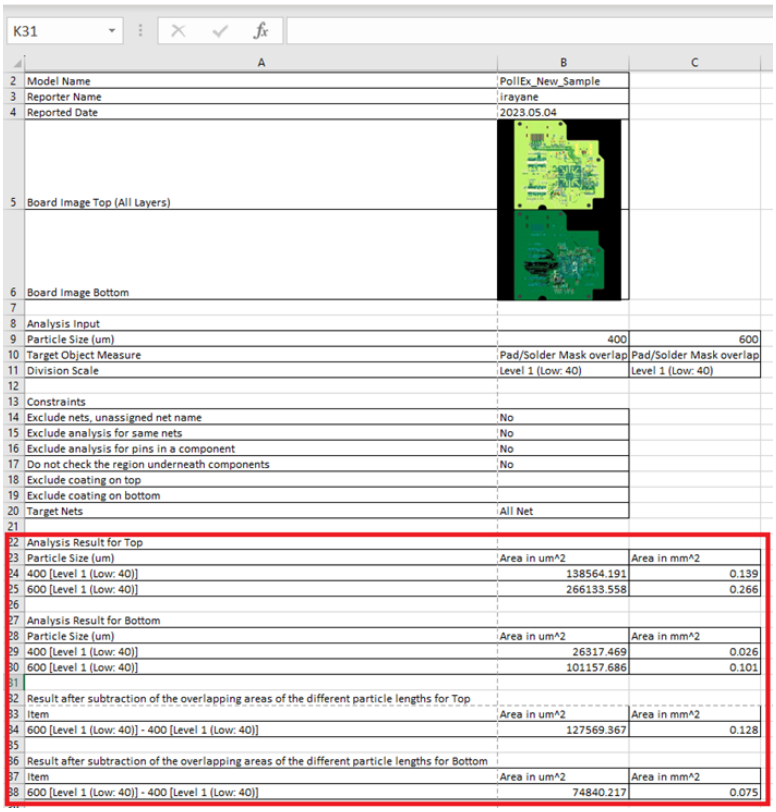


Figure 4 – PollEx Technical Cleanliness Results View

PollEx creates a user layer in which it draws the risk areas between objects for a given particle size. It also calculates the probability of a short by a particle of that size for each of the at-risk object pairs. These probabilities can then be compared to the safety class of the part of the system they affect. If the affected system component is an airbag, for example, there can be no risk, so the design will have to be altered to increase the separation between the affected pins, or the pins must be protected in an effective way—with a coating, for example.

Finally, the user can save the analysis results or export them as a spreadsheet showing each test from the queue, including settings, constraints, and the total critical area for each particle size for the board's top and bottom layers. In addition, the report shows the total area overlap between particle sizes, as highlighted at the bottom of Figure 5.



	A	B	C
2	Model Name	PollEx_New_Sample	
3	Reporter Name	irayane	
4	Reported Date	2023.05.04	
5	Board Image Top (All Layers)		
6	Board Image Bottom		
7			
8	Analysis Input		
9	Particle Size (um)	400	600
10	Target Object Measure	Pad/Solder Mask overlap	Pad/Solder Mask overlap
11	Division Scale	Level 1 (Low: 40)	Level 1 (Low: 40)
12			
13	Constraints		
14	Exclude nets, unassigned net name	No	
15	Exclude analysis for same nets	No	
16	Exclude analysis for pins in a component	No	
17	Do not check the region underneath components	No	
18	Exclude coating on top		
19	Exclude coating on bottom		
20	Target Nets	All Net	
21			
22	Analysis Result for Top		
23	Particle Size (um)	Area in um^2	Area in mm^2
24	400 [Level 1 (Low: 40)]	138564.191	0.139
25	600 [Level 1 (Low: 40)]	266133.558	0.266
26			
27	Analysis Result for Bottom		
28	Particle Size (um)	Area in um^2	Area in mm^2
29	400 [Level 1 (Low: 40)]	26317.469	0.026
30	600 [Level 1 (Low: 40)]	101157.686	0.101
31			
32	Result after subtraction of the overlapping areas of the different particle lengths for Top		
33	Item	Area in um^2	Area in mm^2
34	600 [Level 1 (Low: 40)] - 400 [Level 1 (Low: 40)]	127569.367	0.128
35			
36	Result after subtraction of the overlapping areas of the different particle lengths for Bottom		
37	Item	Area in um^2	Area in mm^2
38	600 [Level 1 (Low: 40)] - 400 [Level 1 (Low: 40)]	74840.217	0.075

Figure 5 – PollEx Technical Cleanliness Results Report

Conclusion

PollEx not only simplifies and automates your PCB design verification, but also greatly reduces cost with these benefits:

- Provides PCB cleanliness classification related to the technical cleanliness standards and regulations
- Improves product safety, reliability, and performance
- Reduces design iterations and product recall risks
- Extends product and PCB lifespan

To view the intuitive PollEx Technical Cleanliness workflow and report navigation in action, see our Technical Cleanliness Overview video.

About Altair PollEx

Altair PollEx is a PCB-level electronic design automation (EDA) software suite covering design review, analysis, and manufacturing. It significantly reduces development cycles while providing a common communication application between schematic engineers, PCB designers, CAE analysts, and manufacturing engineers.

PollEx serves as more than a tool for printed circuit board (PCB) verification. It is a complete PCB verification environment that integrates with existing tool chains—thanks to its use of standard ODP++ formats for PCBs—to accelerate the development of today's smart, connected, and tightly packaged electronic products. PollEx is part of Altair's fully integrated system-level solution that combines mechanical, thermal, electromagnetic, and embedded code design flow with PCB design. Used by global industry leaders, Altair PollEx improves efficiency, product performance, and enhances development collaboration.

To learn more, visit Altair PollEx