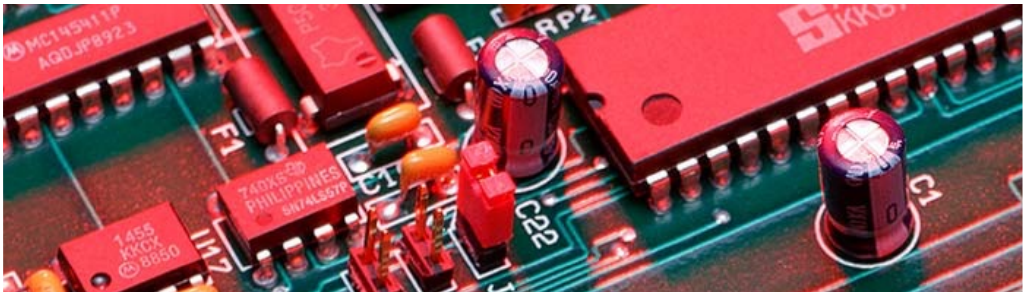
TECHNICAL DOCUMENT

HOW SIMULATING FOR PCB MANUFACTURING DRIVES PROFITABILITY

Smart connected devices are everywhere, in homes, in transportation, and at work. This means electronic system design (ESD) is having a greater influence on almost every type of product requiring new simulation tools to help achieve electronic, electrical, mechanical, thermal, and connectivity goals. New printed circuit board development opportunities also bring new production challenges for manufacturers, who must ensure process efficiency starting with identifying potential defects and optimizing for manufacturing in the design phase.



For any manufacturer, two of the most critical questions around a new product introduction (NPI) are “How do we ensure the quality and consistency of our manufacturing processes?” and “What is the fastest path to profitability?”. Anyone who manufactures printed circuit boards (PCBs) knows that manufacturing is inextricably linked to the company’s bottom line. The discovery of defects can stall development, kick off expensive redesign and testing cycles, and lead to increased warranty claims and damage brand reputation if these issues reach the consumer.

Increasingly, electronics developers are turning to simulation-driven design for manufacturing (SDfM) methods to improve their production efficiency and provide solutions to maximize NPI profit margins.

HOW DOES SIMULATION IMPROVE PRODUCT EFFICIENCY?

Injecting simulation into the PCB development process allows design engineers to identify potential manufacturing and assembly issues early in the R&D phase, before they reach downstream validation and physical testing stages. SDfM provides powerful tools to quickly and accurately recognize common PCB defects that would otherwise require extensive manual review or failed lab or field tests to uncover.

Verification checks are a necessary step to reduce manufacturing cost and delivery time. A comprehensive approach involves electrical validity checks (DFE, DFE+, LDFE) and manufacturing validity (DFM, DFA). However, PCB verification tools alone only go so far to improve production efficiency.

Altair PollEx™ is a solution that accelerates the development of today’s smart, connected, and tightly packaged electronic products. Used by global industry leaders to improve efficiency, increase performance, enable teamwork, and enhance collaboration, it offers tools for full system analysis that integrate mechanical, thermal, electromagnetic, and embedded code design flow with PCB design.

On top of identifying production issues through verification testing, PollEx offers solutions through DFM/DFA analysis including fabrication, assembly, test, flex/rigid-flex, substrate, and panel features. PollEx also exports manufacturing and validation data to production line machinery for fabrication, assembly, and end-of-line testing. PollEx’s end-to-end electronic systems development tools help reduce manufacturing cost and delivery time by optimizing the PCB design for both function and manufacturability.

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WHAT ARE THE MOST COMMON PCB MANUFACTURING ISSUES?

- Acid Traps
- BGA Spacing
- Tombstone Effect
- Test Point Existence
- Visual Features

Acid traps are pocket spaces on the PCB, usually sharp corners, in which etching solution could get trapped. These etching solutions are used to strip excess copper from a board during manufacture. If they are trapped, there is a risk of it tunneling through the board, causing corrosion to the traces and leading to faulty traces.

Common Sources

- Trace bending below 90 degrees most likely acts as acid trap during fabrication, specifically before washing when residual acid gets collected in trap area
- Traces connecting to holes (vias or DIP connections) without teardrops are usually connected at a sharp angle, which could lead to the creation of acid traps

Verification Checks with PollEx

Check for sharp corners for traces: This check looks for patterns that are connected to a pad from a 90-degree angle, helping the user fix routes that will be problematic during etching. This check also helps the user identify if angles are routed in angles other than 45 or 90 degrees by offering a glimpse at all traces flagged as coming into the pad at 90 degrees.

Existence of Teardrops: This check helps determine if a component group is lacking a teardrop, especially for DIP type components where the probability of breakout for vias is possible.

BGA components are a major key to incorporating high-performance ICs into densely populated, complex PCBs. However, there are certain issues that must be considered to ensure proper functionality of the BGA chips. Fixing some of these issues post-manufacturing could prove costly in terms of time and resources.

Common Sources

- The majority of the issues with BGAs are associated with pads for the ball grid under the die
- Proper spacing policy around each BGA pad ensures proper connectivity of the component

Verification Checks with PollEx

Clearance around BGA pads for vias: For the best case BGA routing, the through-hole vias between the BGA pads need to be at the center of 4 BGA pads. In case this is not achieved, that invites a chance of solder applied to BGA pads to scavenge into the vias, since most BGA pads are non-solder mask defined, i.e., solder mask area is larger than metal pad area.

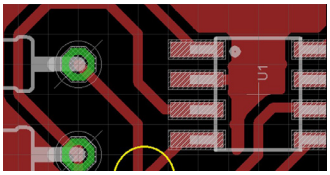
Tombstoning is caused by improper wetting. When the solder paste starts to melt, an imbalanced torque at the ends of the component terminals causes the component to lift from one end.

Common Sources

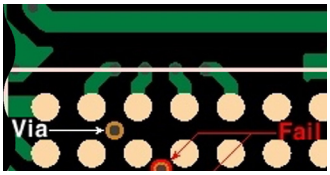
- A difference in connected traces of each pad of a 2-pin device causes difference in soldering time during the reflowing process, which results in a tombstoned component

Verification Checks with PollEx

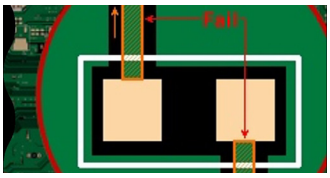
Compare the ratio of connected traces: Due to mismatch in heat dissipating traces between two pads, one pad could require more heat to get a proper connection. Therefore, the temperature difference will generate a wetting force imbalance that causes tombstoning. To prevent tombstoning, ensure the ratio between the connected copper at the pads are within the allowable ratio.



Acid Traps: Altair PollEx checking a PCB for sharp corners and teardrops



BGA Spacing: Altair PollEx being used to confirm clearance around BGA pads for vias



Tombstone Effect: Altair PollEx being used to check for tombstone effect on a PCB, in which a component lifts from one end due to improper wetting

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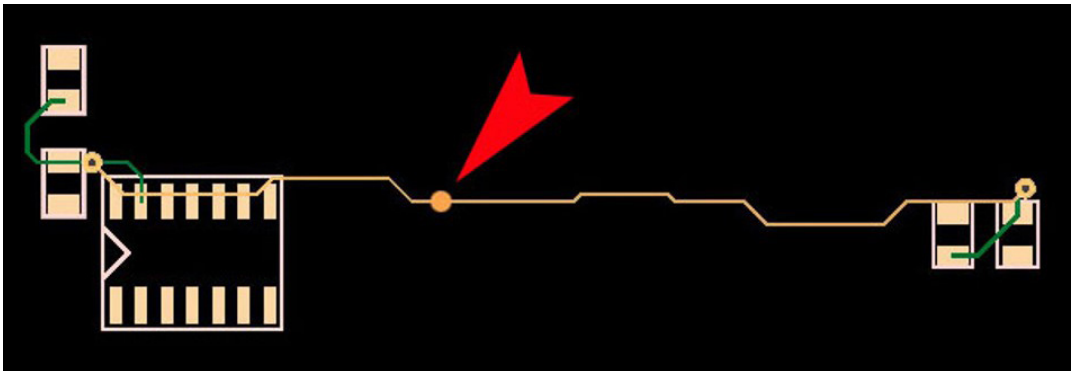


Altair PollEx checking for the existence of test points across PCB nets and components.

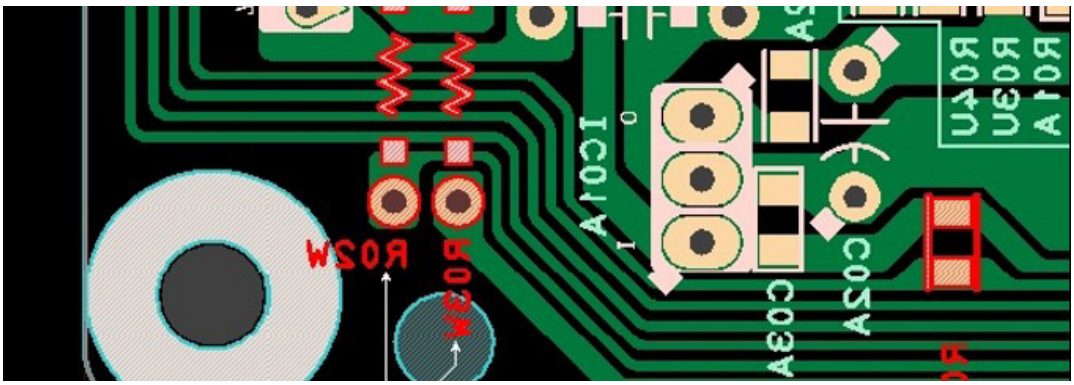
When designing a PCB, it is important to add fixtures for easy testing of vital nets and components. Such testing setups are essential to test objects with minimum or no modification or rework to the design.

Common Sources

- Areas missing test points for difficult to access nets and components or nets associated with power delivery.

Verification Checks with PollEx

Check the existence of test points: Typically test points are incorporated in the design for testing critical nets and components which are associated with power delivery or those with difficulty to access, but some areas may be missed. PollEx checks for the existence of test points for specified components and nets.



Altair PollEx checking PCB visual features for potential layout issues including overlap with objects that may result in performance issues.

When designing a manufacturable PCB, the overlay layers play an important role in the manufacturing process as well as post-manufacturing debug. The overlay layers contain information such as First Pin Mark, Reference Names, and component outlines. It is important to make sure information about these overlay layers is accurately represented to avoid any layout discrepancies.

Common Sources

- For complicated multi-rowed pin ICs, the first pin indicator helps in case of placement as well debugging
- For arrays of passive components, the reference names also provide details for cross-probing with the schematic
- These reference names shouldn't be placed on top of copper areas such as pads and vias, or underneath a component

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Verification Checks with PollEx

Check order of Reference names for arrayed passive components: Reference name ordering for arrayed components should be accurate so that they correlate to the correct component to be placed in the array.

Check existence of first pin mark for complex ICs (components with Reference name "U#"): Marking the first pin for complex ICs helps to avoid errors during the assembly process which could result in components being placed in an incorrect orientation.

Check for reference names overlapping with other objects (components, pads and holes): Reference name should be avoided placed on certain objects on the board to prevent several issues like ink in holes and ink on traces creating SI and PI issues and ink of solderable surfaces, creating bad solder joints.

Sharing Verification Results

Distributing the results of manufacturing verification tests effectively is equally as important as performing the critical checks themselves. PollEx DFx offers a unique export feature that ensures all information from these checks are distributed seamlessly. With custom Excel formatting, users can export and share detailed information with the peripheral teams.

SMT MANUFACTURING GUIDANCE

Surface-mount technology (SMT) is a method in which electrical components are mounted directly onto the surface of a printed circuit board. In order to ensure manufacturing efficiency, SMT process engineers need to be able to generate manufacturing data easily starting at PCB design data review.

PollEx provides an efficient working environment for SMT process engineers to generate data from the screen printer, mounter, soldering, test, and router. Below are a few examples of tools in PollEx geared toward improving efficiency for process engineers.

Metal Mask Manager

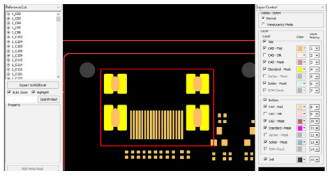
- Registers standard metal mask database, manages metal mask changing history, and check differences between design and standard data mask
- Change design's metal mask according to standard metal mask
- Manage several different metal mask databases

Block JIG Generator

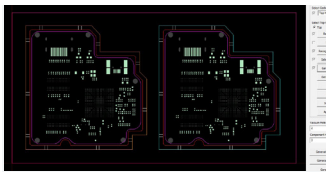
- Stable supporting for the bare PCB and evenly applies lead in the screen printer equipment that prints the solder cream during the SMD process
- JIG should be repeatedly designed and manufactured as the shape of the PCB changes
- Quickly generate design drawing for manufacturing JIG using PCB design data and panel PCB Gerber or array board

Mounting Emulator

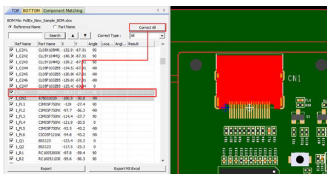
- Mounter assembly checking toolset based on 3D package part libraries constructed with UPE
- Check part information and analyze part placement coordinates and angle
- Correct part location and angle differences
- Export customized Microsoft Excel results



Metal mask manager in Altair PollEx being used to manage changes to the PCB metal mask design and compare to a database of standard metal masks



Altair PollEx's Block JIG generator being used to verify the manufacturability of PCBs from the perspective of the screen printing equipment



Mounting emulator tools in Altair PollEx make verification of proper PCB mounting fast and easy

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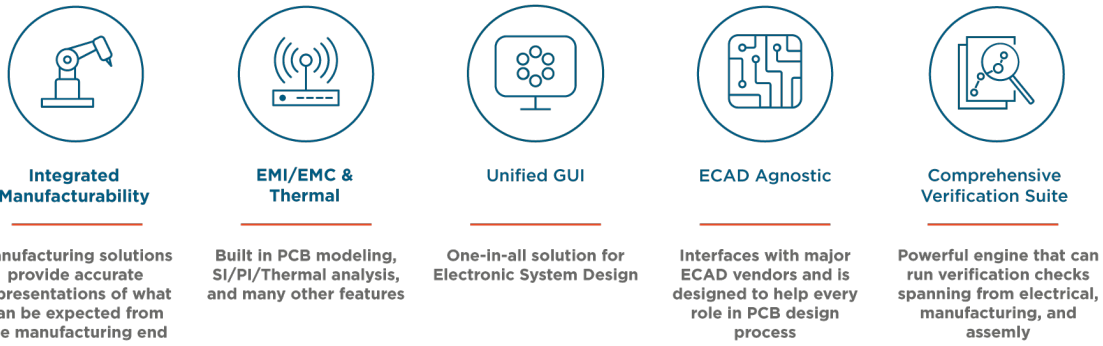
WORKING WITH ALTAIR

Delivering electronics that delight consumers requires more than just linking the ECAD and MCAD worlds. It requires physics-based analysis at the speed of design and collaboration across disciplines throughout development. PollEx brings Altair's simulation-driven design philosophy to the electronics industry, inspiring innovation while ensuring timing, performance, reliability, and compliance targets are met



Altair PollEx delivers a comprehensive set of tools for electronic system design, including integrated manufacturability, EMI/EMC & Thermal, a unified GUI with an ECAD agnostic environment, and a comprehensive verification suite.

With smart connected devices everywhere, in homes, in transportation, and at work, and this means electronic system design (ESD) is having a greater influence on almost every type of product. New simulation tools are needed to help achieve the electronic, electrical, mechanical, thermal, and connectivity goals of today's electronics manufacturers. Altair's simulation-driven design tools enable your team of specialized engineers to collaborate across all aspects of printed circuit board development from concept to manufacturing. Our products streamline your process, eliminate design iterations, and reduce time-to-market.

Learn more at altair.com/electronic-system-design

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